Post-doctoral position

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Field:

Chemistry for nanos	☐	Molecular electronics	☐	Process Technologies	☐
Imaging devices & Systems	☐	Nanocharacterization	☐	RF Devices & Systems	☐
Materials	☐	Nanoelectronics	☐	Spintronics	☐
Memory technologies	☒	Nanos for Energy	☐	Other	☒
MEMS and sensors	☐	Nanoscale simulation	☐	Algorithm & compiler	☒
Microtechnologies for bio	☐	Photonics	☐	Computing architecture	☒

Required	Duration	Start		
PhD	18 months	From Dec. 2016		

Topic: Micro-programming optimization of "in-memory computing" circuits

Context:

The concept of "in-memory computing", which consists in bringing computation tasks inside the memory macro, is a novel and promising approach where we need to explore new computing algorithms and methodologies. This approach differs in particular from those known as "processing-in-memory" (PIM) that aim at moving computation elements near the memories (especially DRAM) without changing their internal architecture. Our approach called DRC² (*Dynamically Reconfigurable Computing Circuit*) consists in adapting conventional memory peripheral circuits (I/O, address decoder, ...) to perform logic (AND, OR, XOR, ...) and arithmetic (addition/subtraction, ...) operations inside the memory macro (SRAM or NVM), as shown in Figure 1.

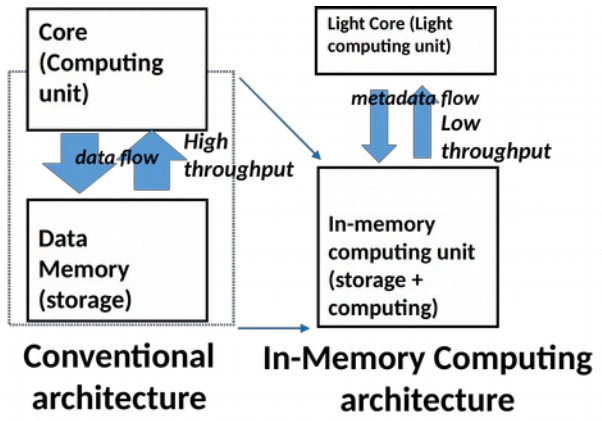

Figure 1: Illustration of conventional computing unit and the working memory (aka « Von Neumann » or « Harvard ») versus the proposed computing architecture (aka « in-memory computing »)

The first objective of the post-doctoral researcher is to identify key applications in the field of data processing (e.g. imaging, cryptography...) that can take a full advantage of the proposed memory-based computation circuit with an appropriate computing model. Since the invention of the microprocessor in the 70's, the computation units are still physically separate from working memories and this limits the computing throughput (leading the famous "memory wall") and generates huge electrical consumption and latencies due to the Von Neumann architecture model. The proposed computing circuit enables performing simple arithmetic and logic operations in the same time keeping the data inside the memory circuit. Combined with a dedicated programming approach, it will therefore enable reducing significantly power consumption related to the data transfer in a chip, while increasing the throughput for demanding applications.

Keywords: *in-memory computing*, *micro-programming*, *micro-architecture*, *image/video processing*, *circuit design*

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Study:

We are looking to recruit a highly motivated post-doctoral researcher to develop an optimized micro programming environment for an "in-memory computing" circuit based on DRC² concept. He/she will interact with both circuit design and software teams to propose an efficient architecture and software tools. More precisely, he/she will:

- Perform a bibliography on potential applications and dedicated programming languages.
- Select key applications and propose an architecture based on DRC² to take advantage of the DRC² capabilities.
- Develop system-level testbenches to evaluate speed and power enhancements compared to existing solutions.
- Interact with circuit design team in order to finely understand the DRC² concept.
- Help to develop a testchip based on DRC² concept driven by a specific set of instructions. The final output will be the electrical validation of a testchip.

Such a co-optimization, i.e. a continuous feedback between design and software teams, is crucial and required for project success.

Required skills:

- Compilers: memory models, tools for parallelism extraction, low level parallelism, low level code generation, …
- Knowledge on algorithm
- Computing architecture: instruction set architecture, memory hierarchy, vector architecture, …
- Collaboration between design team and compiler team

Appreciated skills:

- Knowledge in circuit design (digital and/or full custom)
- Writing skills for academic publications

Lab

Institute/Department/Section/Laboratory	DRT/LETI/DACLE/SCSN/LISAN CTReg/DPACA/LSAS DRT/LIST/DACLE/SCSN/LIALP
Address	CEA/GRENOBLE 17 rue des Martyrs 38054 Grenoble CEDEX 9 France

Supervisors		
GIRAUD Bastien (memory design) FOURNIER Jacques CHARLES Henri-Pierre	Phone: +33 (0)4 38 78 17 58	E-mail: bastien.giraud@cea.fr